

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE PATENT OPERATION

In re the Application of: HIRAOKA, Tetsuya, et al.

Date Allowed: January 30, 2004

Serial Number: 09/973,002 Examiner: Lourdes C. Cruz

Filed: October 10, 2001 Group Art Unit: 2827

P.T.O. Confirmation No.: 4785

For. SEMICONDUCTOR DEVICE WITH STACK OF SEMICONDUCTOR CHIPS

POWER TO FILE CORRECTED FORMAL DRAWINGS

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Date: Loburary 20, 2004

Sir:

The undersigned, attorney of record in the above-identified application, hereby instructs Frankie Locklear and Element Patent Drafting, to correct the drawings, as required and approved in such above-identified application and to file such corrected formal drawings in the United States Patent and Trademark Office in such application.

In the event that this paper and such formal drawings are not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fee which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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